UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,521	07/14/2003	Qing Deng	10003809-7	7465

7590 10/07/2005

AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, CO 80537-0599

EXAMINER	
VAN ROY, TOD THOMAS	
ART UNIT	**PAPER NUMBER**
2828	

DATE MAILED: 10/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,521	DENG ET AL.	
	Examiner	Art Unit	
	Tod T. Van Roy	2828	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *47,48,50-55 and 57-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47,48,50-55 and 57-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 47 and 54 have been considered but are moot in view of the new ground(s) of rejection. Please see the rejection to follow.

Applicant's arguments, see Remarks, filed 08/02/2005, with respect to the rejection(s) of claim(s) 48 and 55 under U.S.C 103(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art.

Applicant's arguments, see Remarks, filed 08/02/2005, with respect to the rejection(s) of claim(s) 50-52 and 57-59 under U.S.C 103(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art.

Applicant's arguments with respect to claims 53 and 60 have been considered but are moot in view of the new ground(s) of rejection. Please see the rejection to follow.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 47, and 54 are rejected under 35 U.S.C. 102(b) as being anticipated by Ramdani et al. (US 5835521).

With respect to claim 47, Ramdani discloses a VCSEL (fig.3) comprising a first mirror stack (fig.3 #13), a second mirror stack (fig.3 #42) a cavity region disposed between the first mirror stack and the second mirror stack (fig.3 #34,42,13), wherein the first mirror stack, the cavity region, and the second mirror stack are arranged along a vertical direction (fig.3), and the cavity region includes, active region (fig.3 #34), a first side facing the first mirror stack (first side face on upper side, near top of paper, of active region #34), and a second side facing the second mirror stack (2^{nd} side face on upper side, near bottom of paper, of active region #34); a defect source (col.5 lines 45-52, emphasis on lines 50-52) located such that only one of the first and second sides of the cavity region faces the defect source (first side faces it, since the defect is also found to be on top of and next to layer #28, col.5 lines 45-52); and a reliability-enhancing layer (fig.3 #31, col.5 lines 9-10) positioned within the defect source to reduce migration of defects in the vertical direction from the defect source to the active region (would reduce defects transitioning from the first side, vertically, down to the active region), whereby the reliability enhancing layer reduces defect induced degradation of the active region by the defect source.

With respect to claim 54, Ramdani discloses a method of manufacturing a VCSEL comprising forming a first mirror stack (col.3 lines 26-33), a second mirror stack

(col.6 lines 4-6) a cavity region disposed between (fig.3 #34,42,13), wherein the first mirror stack, the cavity region, and the second mirror stack are arranged along a vertical direction (fig.3) and the cavity region includes an active region (col.5 lines 11-13), a first side facing the first mirror stack (first side face on upper side, near top of paper, of active region #34), and a second side facing the second mirror stack (2nd side face on upper side, near bottom of paper, of active region #34); forming a defect source (col.5 lines 45-52, emphasis on lines 50-52) located such that only one of the first and second sides of the cavity region faces the defect source (first side faces it, since the defect is also found to be on top of and next to layer #28, col.5 lines 45-52), and a reliability-enhancing layer positioned within the defect source to reduce migration of defects in the vertical direction from the defect source to the active region (would reduce defects transitioning from the first side, vertically, down to the active region), whereby the reliability enhancing layer reduces defect induced degradation of the active region by the defect source.

Claims 48, 50-51, 53, 55, 57-58,60-61, and 63 are rejected under 35 U.S.C. 102(b) as being anticipated by Choquette et al. (US 5493577).

With respect to claim 48, Choquette discloses the claimed VCSEL (fig.3) comprising a first mirror stack (fig.3 #14), a second mirror stack (fig.3 #16), a cavity region disposed between the first mirror stack and the second mirror stack (fig.3 #32,30,32) including an active region (fig.3 #30), a defect source (fig.3 #20), and a reliability-enhancing layer (col.12-13 lines 66-20) positioned with respect to the defect

source to reduce defect induced degradation of the active region by the defect source (col.13 lines 8-11), where the defect source is disposed between the reliability-enhancing layer and the cavity region (two reliability enhancing layers, above and below defect, so the defect source is disposed between the upper reliability layer and the cavity); and a second reliability-enhancing layer separated from the first reliability-enhancing layer by one or more other layers (two reliability enhancing layers, above and below defect, so the defect source is the layer separating the reliability layers), wherein the first and second reliability-enhancing layers are located on opposite sides of the defect source.

With respect to claims 50-51 and 61, Choquette discloses the claimed VCSEL (fig.3) comprising a first mirror stack (fig.3 #14), a second mirror stack (fig.3 #16), a cavity region disposed between the first mirror stack and the second mirror stack (fig.3 #32,30,32) including an active region (fig.3 #30), a defect source (fig.3 #20), and a reliability-enhancing layer (col.12-13 lines 66-20, adjacent-two reliability enhancing layers, above and below defect) positioned with respect to the defect source to reduce defect induced degradation of one or more VCSEL regions, wherein the reliability-enhancing layer is configured to at least in part balance strain created by the defect source (col.13 lines 8-11, wherein the oxide growth would induce a compressive strain due to the increased thickness, and the offsetting strain by the reliability layers would then inherently be tensile).

With respect to claim 53, Choquette discloses the claimed VCSEL (fig.3) comprising a first mirror stack (fig.3 #14), a second mirror stack (fig.3 #16), a cavity

region disposed between the first mirror stack and the second mirror stack (fig.3 #32,30,32) including an active region (fig.3 #30), a defect source (fig.3 #20), and a reliability-enhancing layer (col.12-13 lines 66-20) positioned with respect to the defect source to reduce defect induced degradation of one or more VCSEL regions, wherein the defect source creates a concentration gradient inducing defect migration, and the reliability-enhancing layer introduces strain that reduces the induced defect migration (col.13 lines 8-11).

With respect to claim 55, Choquette discloses a method of manufacturing a VCSEL comprising forming a first mirror stack, a second mirror stack, and a cavity region disposed there between, wherein the cavity region includes an active region (col.5 lines 9-28), forming a defect source (col.9 lines 7-13), forming a reliability-enhancing layer (col.12-13 lines 66-20) positioned with respect to the defect source to reduce defect induced degradation of the active region by the defect source (col.13 lines 8-11), where the defect source is disposed between the reliability-enhancing layer and the cavity region (two reliability enhancing layers, above and below defect, so the defect source is disposed between the upper reliability layer and the cavity); and a second reliability-enhancing layer separated from the first reliability-enhancing layer by one or more other layers (two reliability enhancing layers, above and below defect, so the defect source is the layer separating the reliability layers), wherein the first and second reliability-enhancing layers are located on opposite sides of the defect source.

With respect to claims 57-58 and 63, Choquette discloses a method of manufacturing a VCSEL comprising forming a first mirror stack, a second mirror stack,

and a cavity region disposed there between, wherein the cavity region includes an active region (col.5 lines 9-28), forming a defect source (col.9 lines 7-13), forming a reliability-enhancing layer (col.12-13 lines 66-20, adjacent-two reliability enhancing layers, above and below defect) positioned with respect to the defect source to reduce defect induced degradation of one or more VCSEL regions, wherein the reliability-enhancing layer is configured to at least in part balance strain created by the defect source (col.13 lines 8-11, wherein the oxide growth would induce a compressive strain due to the increased thickness, and the offsetting strain by the reliability layers would then inherently be tensile).

With respect to claim 60, Choquette discloses a method of manufacturing a VCSEL comprising forming a first mirror stack, a second mirror stack, and a cavity region disposed there between, wherein the cavity region includes an active region (col.5 lines 9-28), forming a defect source (col.9 lines 7-13), forming a reliability-enhancing layer (col.12-13 lines 66-20) positioned with respect to the defect source to reduce defect induced degradation of one or more VCSEL regions, wherein the defect source creates a concentration gradient inducing defect migration, and the reliability-enhancing layer introduces strain that reduces the induced defect migration (col.13 lines 8-11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 52 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choquette in view of Shieh.

With respect to claims 52 and 59, Choquette teaches the VCSEL outlined in rejection of claim 50 above, comprising a first mirror stack comprising layers of oxidized AlGaAs (col.9 lines 11-12), and a reliability enhancing layer which reduces strain and degradation effects in the active region (col.13 lines 8-11). Choquette does not teach the layer to be made of InxGa1-xP. Shieh teaches a reliability enhancing layer made of InGaP that reduces strain and degradation effects in the active region (col.3 lines 10-15). Neither source teaches that x should be less than .5 tensile. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the

reliability enhancing layer of Choquette with the reliability enhancing layer material type of Shieh as an obvious design choice to fit the material system which is being worked with; in addition it would have been obvious to use x less than .5 tensile as it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 47-48, 50-55, and 57-66 rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3, 6, 16-20, 29-30, 34, and 43-46 of U.S. Patent No. 6628694. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims in the current application are broader than the claims of patent '694 and hence '694 then outlines an existing embodiment of the claims of the application under review.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tod T. Van Roy whose telephone number is (571)272-8447. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571)272-1835. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVR

MINSUN OH HARVEY
PRIMARY EXAMINER